LAYOUT DESIGN PRACTICES AROUND THE OUTPUT OF AN ON-CHIP DC-DC CONVERTER

1. Introduction

The aim of this document is to show what layout design practices should be applied around the output of an on-chip DC-DC converter. When layout is not carefully designed around the DC-DC converter, it can cause the interference leakage to get to critical parts of the radio and create damage in RF performance.

2. DC-DC Converter Circuit

The diagram of a typical boost converter circuit can be seen on the following figure:

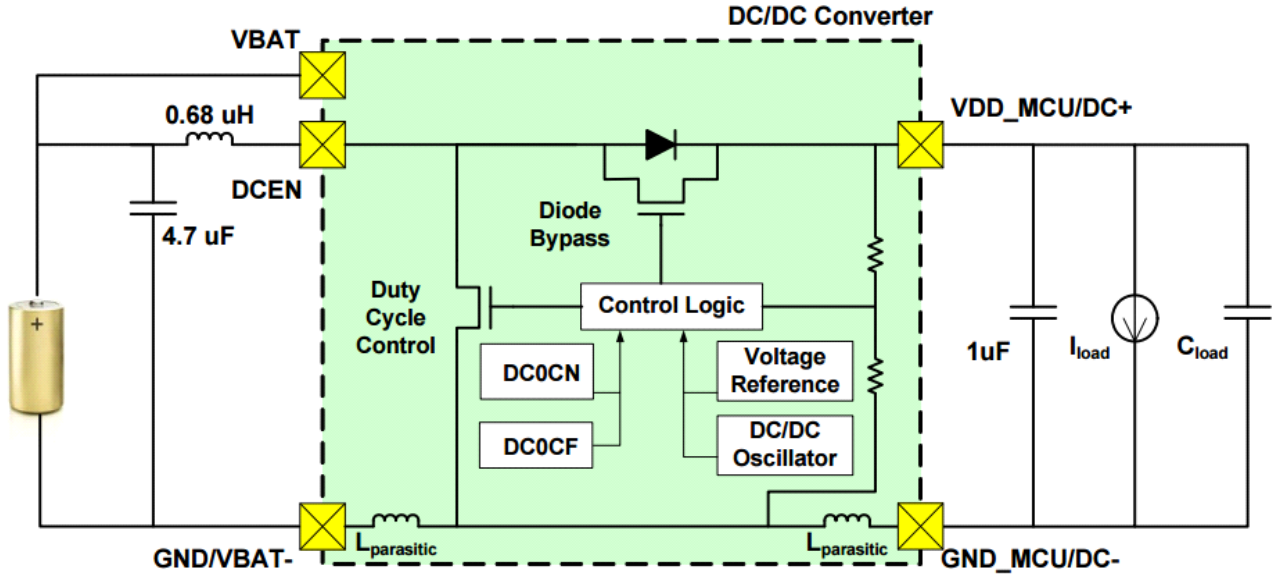

Figure 1. Boost Converter Circuit

The step up conversion of the input DC voltage is realized by the switching of the Duty Cycle Control and Diode Bypass switches.

Although in this document the boost converter is shown in detail, similar layout practices should be considered when designing a buck converter circuit.

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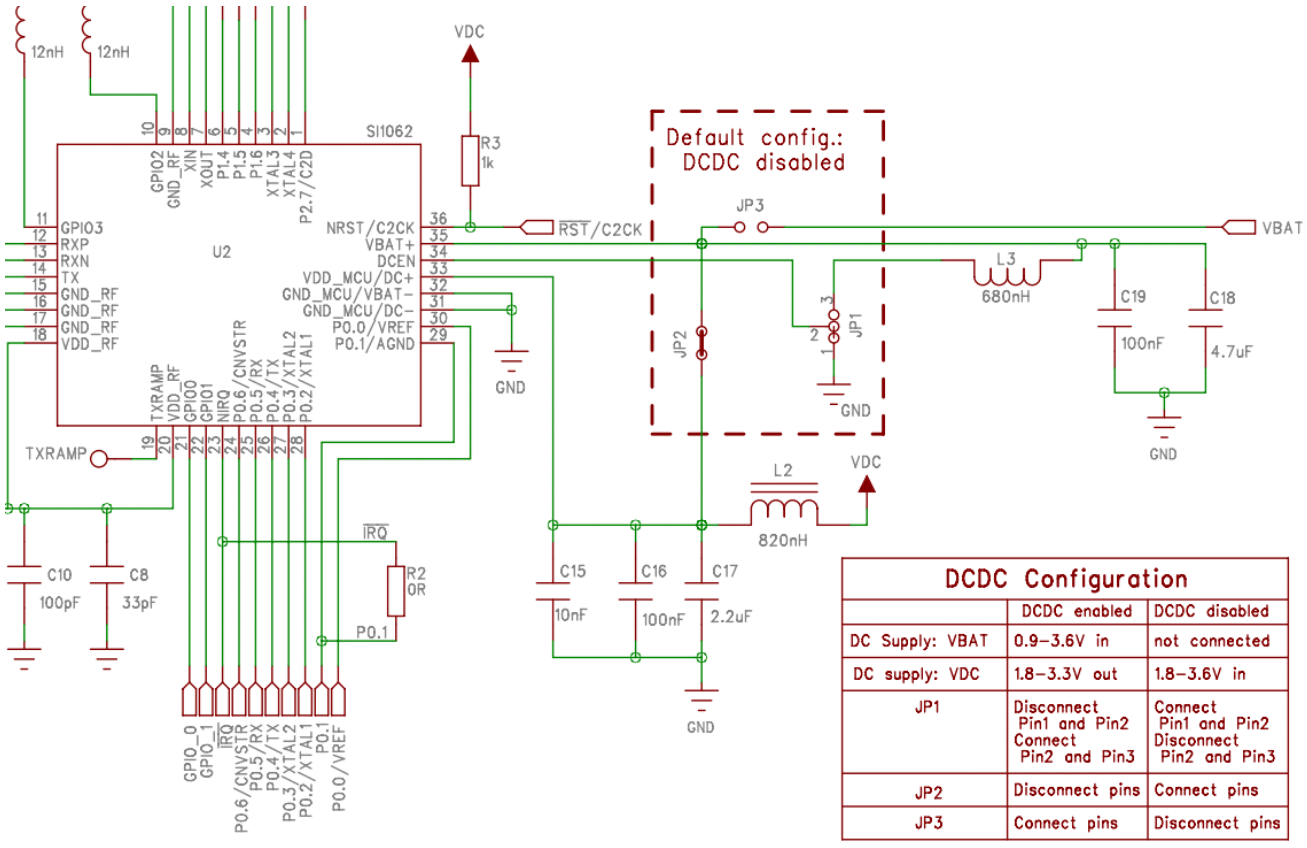
3. Layout Recommendations Around the DC-DC Converter Output

The main points to be aware of when designing the layout around the DC-DC converter are listed below:

- Make sure all the VDD pins of the chip are filtered individually with capacitors placed close to the related pins. If the VDD lines with poor filtering are close to the DC-DC converter output, interfering signals caused by voltage fluctuation of the DC-DC converter can get to these lines.
- Jamming signal on the VDD is dangerous as it will spread out everywhere inside the chip.
- Due to the far situated filter capacitors, the interference current travels on many long paths through the board, and gets back to the IC ground on a difficult way.
- Long interference leakage paths on the PCB are dangerous in TX mode as these traces may behave as hidden antennas and cause unwanted emissions and violation of the radiation standards.
- Many vias should be used around the output of the DC-DC converter. With missing vias to the ground, the ground plane does not work as a real unified ground anymore, and as some parts work as a patch antenna and radiate, potentially causing again violation of the emission standards.
- The leakage paths can cause the radio chip not to see a good ground reference (i.e. interference can be observed), and this may cause damage in RF performance (lower TX power, higher TX harmonics, higher current consumption, RX sensitivity loss).
- If there is any GND pin close to the VDC pin on the chip, it should be connected to the GND pins of all the nearby filtering capacitors using many vias.
- The layer beneath the layer where the chip with internal DC-DC converter is placed (basically the top layer) should be an equal ground layer, and should be disconnected by traces only if necessary.



DCDC Configuration		
	DCDC enabled	DCDC disabled
DC Supply: VBAT	0.9–3.6V in	not connected
DC supply: VDC	1.8–3.3V out	1.8–3.6V in
JP1	Disconnect Pin1 and Pin2 Connect Pin2 and Pin3	Connect Pin1 and Pin2 Disconnect Pin2 and Pin3
JP2	Disconnect pins	Connect pins
JP3	Connect pins	Disconnect pins

Figure 2. Reference Design Schematic with Built-in DC-DC Converter

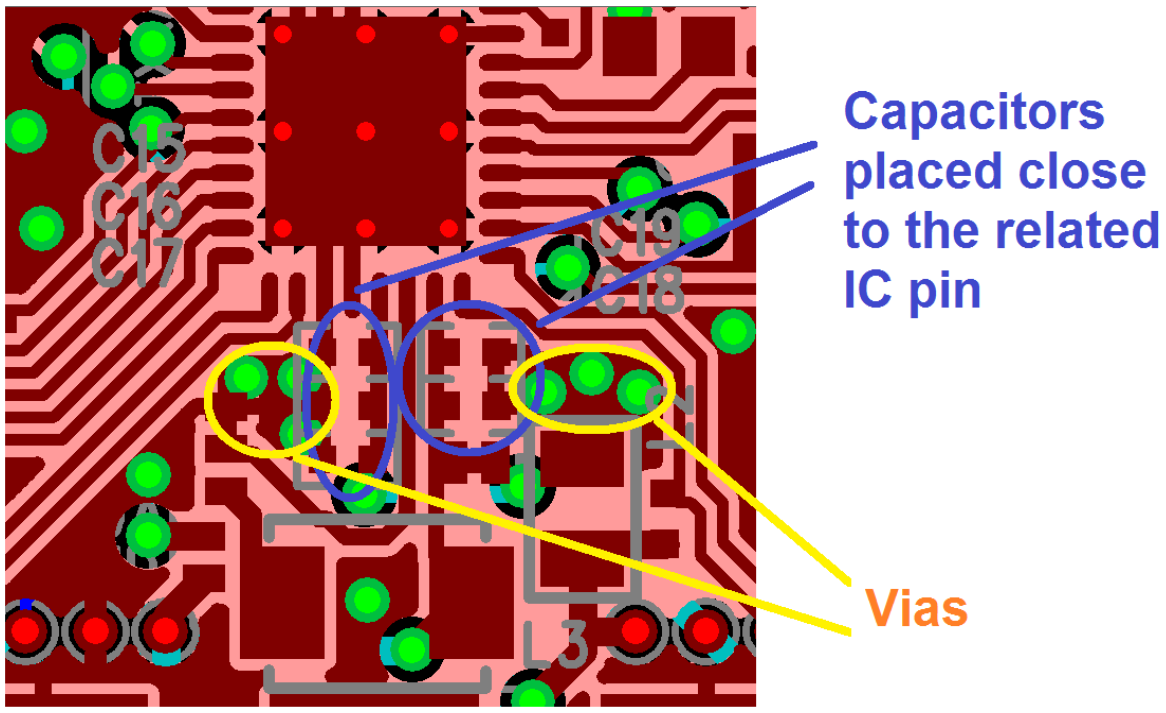


Figure 3. DC-DC Converter Output of the Reference Design Layout

A reference design layout using a DC-DC converter can be seen on Figure 3. All the parallel filtering capacitors are connected to the ground with many vias, and are placed close to the related IC pin.

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